Atty. Docket No. OPP-GZ-2007-0022-US
Serial No: 10/736,063

Amendments to the Claims

Please amend Claim 1, cancel Claims 12 and 20, and add new Claims 24-25 as shown below. This listing of Claims replaces all prior versions and listings of the Claims in this application.

1. (Currently Amended) A method of forming [[a]] gates in a semiconductor device, the method comprising:

forming a shallow trench isolation (STI) to define an active region in a semiconductor substrate;

forming a gate oxide layer on the semiconductor substrate;

~~forming on the semiconductor substrate~~depositing a sacrificial layer on the semiconductor substrate to a thickness that determines a width of the gates;

selectively etching the sacrificial layer to form a sidewall opening over the active region of the semiconductor substrate and the STI until the gate oxide is exposed;

forming a polycrystalline silicon layer on an area of the gate oxide layer exposed through the sidewall opening and on the sacrificial layer;

anisotropically etching the polycrystalline silicon layer such that ~~sidewall~~the gates remain on sidewalls of the sidewall opening, the ~~sidewall~~ gates having ~~a minimum~~the width; and

removing the sacrificial layer.

2. (Original) A method as defined by claim 1, wherein the sacrificial layer comprises a nitride layer.

3. (Previously Presented) A method as defined by of claim 2, wherein removing the nitride layer comprises a wet etching process.

4. (Previously Presented) A method as defined by claim 1, wherein removing the sacrificial layer comprises a wet etching process.

5. (Previously Presented) A method as defined by claim 1, wherein anisotropically etching the polycrystalline layer comprises an etch-back process.

6. (Previously Presented) A method as defined by claim 1, wherein a thickness of the sacrificial layer determines widths of the sidewall gates.

7. (Previously Presented) A method as defined by claim 1, wherein the width of the sidewall opening corresponds to a distance from one gate to an adjacent gate.

8. (Original) A method as defined by claim 7, wherein the sacrificial layer comprises a nitride layer.

9. (Previously Presented) A method as defined by claim 8, wherein removing the nitride layer comprises a wet etching process.

10. (Previously Presented) A method as defined by claim 7, wherein removing the sacrificial layer comprises a wet etching process.

11. (Previously Presented) A method as defined by claim 7, wherein anisotropically etching the polycrystalline layer comprises an etch-back process.

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Previously Presented) The method of claim 5, wherein the etch-back process comprises over etching the sidewall gates to the minimum width.

17. (Previously Presented) The method of claim 11, wherein the etch-back process comprises over etching the sidewall gates to the minimum width.

18. (Previously Presented) The method of claim 1, further comprising depositing a photoresist layer on the sacrificial layer.

19. (Previously Presented) The method of claim 18, further comprising patterning the photoresist layer to form an opening exposing a predetermined area of the sacrificial layer.

20. (Cancelled)

21. (Previously Presented) The method of claim 19, wherein the opening encompasses an area on the substrate from where one sidewall gate will be formed to where an adjacent gate will be formed.

22. (Previously Presented) The method of claim 1, wherein forming the STI defines a plurality of active regions in the substrate, and etching the sacrificial layer forms an opening over at least two of the active regions and the STI.

23. (Previously Presented) The method of claim 1, wherein etching the sacrificial layer exposes the active region and the STI.

24. (New) The method of Claim 1, wherein anisotropically etching the polycrystalline silicon layer forms first and second sidewall gates on respective first and second sidewalls of the sacrificial layer and removes polycrystalline silicon above said STI and first and second portions of said substrate adjacent to said STI, said first and second portions of said substrate being between said STI and respective portions of said substrate below said first and second sidewall gates.

25. (New) The method of Claim 1, wherein anisotropically etching the polycrystalline silicon layer further comprises an over-etch.